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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,125	06/29/2001	Shunpei Yamazaki	740756-2330	7248
31780	7590	02/28/2006	EXAMINER	
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			KEBEDE, BROOK	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Advisory Action
Before the Filing of an Appeal Brief**

Application No.

09/894,125

Applicant(s)

YAMAZAKI ET AL.

Examiner

Brook Kebede

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--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 09 February 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: (See the attachment). (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: 1-17, 19-30 and 47-58.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____.
13. ☐ Other: _____.

Brook Kebede
Brook Kebede
Primary Examiner
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Continuation Sheet (PTO-303)

Advisory Action

1. On cursory consideration, the request for reconsideration and the proposed amendment, which has been entered, does not clearly appear to overcome the rejections.

Response to Arguments

2. Applicants' arguments filed on February 9, 2006 have been fully considered but they are not persuasive.

With respect to claims rejection under 35 U.S.C. § 103, applicants argue that "the prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Independent claims 1-12, 19, 20; 47 and 48 recite leveling a surface of a semiconductor film by recrystallizing a semiconductor film after removing irradiation of a laser light and removal of an oxide film. For the reasons provided below, Morosawa, Hara, Kudo and Yamazaki '232, either alone or in combination, do not teach or suggest the above-referenced features of the present invention..."

In response to applicants' argument it is respectfully submitted that the combination of Morosawa and Hara et al. disclose all the claimed limitations of claims 19, 20, 23-30, 47, 48 and 51-58 as applied in Paragraph 2 of the Office action of November 7, 2005.

The difference between the Morosawa and the instant application claimed invention, i.e., particularly for claims 19, 25, 27 and 29, is that the instant application is claimed *recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process* whereas Morosawa is silent about the *recrystallizing the semiconductor film* Morosawa discloses *removing of the native oxide layer* by cleaning. As clearly indicated in the Office action

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that was mailed on November 7, 2005, both Morosawa and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa and Hara et al. are analogous. Hence, it would have been within the scope of ordinary skill in the art to combine the teachings of Morosawa and Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability because one having ordinary skill in the art would have been motivated to look to analogous art teaching suitable or useful methods for performing recrystallizing the semiconductor film in order to produce a semiconductor device having semiconductor thin film with good uniformity and high reliability because such process is recognized by Hara et al. for its suitability of an intended purpose.

Further, applicants argue that "Hara appears to teach "a method and an apparatus for fabricating a thin film semiconductor device, capable of providing a clean and high-quality semiconductor/insulator interface" without exposing the polycrystalline Si thin film to the outside air in order to solve a problem of forming a native oxide film on a surface of the polycrystalline Si thin film (column 1, line 50 to column 2, line 5; and column 8, lines 19-22). That is, Hara seeks to avoid production of a native oxide film on a surface of a polycrystalline Si thin film. Therefore, the Applicants respectfully submit that Hara cannot teach or suggest leveling a surface of a semiconductor film by recrystallizing a semiconductor film after irradiation of a laser light and removal of an oxide film..."

In response applicants' contention, it is respectfully submitted that both Morosawa and Hara et al. disclosure recognize avoiding contamination on the surface of the semiconductor thin film due to oxygen build up on the surface of the semiconductor (i.e., silicon) thin film. This is

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an art recognized problem and both have different way of dealing with it. The main issue the semiconductor thin film is still undergoes different types of cleaning process during the fabrication of TFTs and in order to avoid damage on the surface and formation of dangling bond (i.e., art recognized term for defect in the bond, when an atom is missing a neighbor to which it would be able to bind which disrupt flow of electrons in the thin film silicon). Therefore, recrystallizing for the semiconductor film by irradiation of a laser light in order to avoid such problem as disclosed Hara et al. does not teach away the disclosure of Morosawa it rather supports Morosawa quest avoiding of the dangling bond.

Furthermore, the motivation to combine Morosawa and Hara et al. can be found in Hara et al. reference in Col. 1, lines 65 -- Col. 2, line 49). The strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. See *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983). Therefore, recrystallizing the semiconductor film (i.e., the silicon thin film) after cleaning (i.e., the cleaning process that removed native oxide layer as suggested by Morosawa and the clean surface that suggested by Hara et al.) in presence of hydrogen atom is beneficial to avoid formation of dangling bond thereby forming the semiconductor film having good uniformity and high reliability.

Applicants further argue that “Kudo and Yamazaki '232 do not cure the above-referenced deficiencies in Morosawa and Hara. Kudo is relied upon to allegedly teach laser irradiation in air, and Yamazaki '232 is relied upon to allegedly teach furnace annealing. However, Morosawa, Hara, Kudo and Yamazaki '232, either alone or in combination, do not teach or suggest leveling

a surface of a semiconductor film by recrystallizing a semiconductor film after removing irradiation of a laser light and removal of an oxide film. Since Morosawa, Hara, Kudo and Yamazaki '232 do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained...”

In response to applicants’ argument, it is respectfully submitted that the combination of Morosawa and Hara et al. is proper as shown herein above. In addition, the combination Morosawa, Hara et al. and Yamazaki et al. is still proper because the use of furnace annealing is rather alternative heating process to that of the laser annealing. Both laser and furnace annealing have its own advantage as well as disadvantages depending upon the process requirement. However, it is available to one having ordinary skill to apply it depending its suitability. In this regard, the instant application claimed invention use both furnace annealing and laser annealing alternatively. Therefore, alternative use of process for similar intend purpose and result does not amount the references are not combinable. “The prior art’s mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...” See *In re Fulton*, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Correspondence

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
February 21, 2006